Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ATSUSHI MIYANISHI and HISASHI MATSUMOTO

Appeal No. 2003-2132
Application 09/114,203

ON BRIEF

Before KIMLIN, GARRIS and OWENS, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from the final rejection of claims 13-24. Claims 2, 3 and 6-11, which are all of the other claims pending in the application, stand withdrawn from consideration by the examiner as claiming a nonelected invention.

THE INVENTION

The appellants claim a semiconductor device and a method for making it. Claim 13, directed toward the semiconductor device, is illustrative:

13. A semiconductor device comprising:

an active area with at least one MOS transistor to be formed therein; and

an insulation film for defining said active area,

said active area having a recess in plan configuration,

said recess being defined by first, second and third edges,

said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend,

said active area having a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said at least one MOS transistor including

a first MOS transistor having a first gate electrode, and

a second MOS transistor having a second gate electrode,

said first gate electrode extending in a direction perpendicular to the direction in which said fourth edge extends, said first gate electrode having a first end extending beyond said fourth edge over said insulation film,

said second gate electrode extending in a direction perpendicular to the direction in which said third edge extends, said second gate electrode having a first end extending beyond said third edge over said insulation film,

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, the length of said second gate electrode being greater than the length of said first gate electrode.

THE REFERENCES

Jassowski	5,668,389	Sep. 16, 1997
Shou et al. (Shou)	5,811,859	Sep. 22, 1998
	(effective filing date	Sep. 29, 1995)
Bergemont (PCT application)	WO 94/29898	Dec. 22, 1994

THE REJECTIONS

The claims stand rejected under 35 U.S.C. § 103 as follows: claims 13, 17-19, 23 and 24 over Shou in view of Bergemont, and claims 14-16 and 20-22 over Shou in view of Bergemont and Jassowski.[1]

OPINION

We affirm the aforementioned rejections.[2]

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[1] The examiner points out that the inclusion of claim 23 in the rejection over Shou in view of Bergemont and Jassowski in the final rejection was a typographical error (answer, page 3).

[2] We incorporate herein the examiner's explanations of the rejections and responses to the appellants' arguments.

The appellants state that the claims are separately patentable (brief, page 6). We discuss the claims separately to the extent justified by the appellants' arguments. *See In re Burckel*, 592 F.2d 1175, 1178-79, 201 USPQ 67, 70 (CCPA 1979); *In re Herbert*, 461 F.2d 1390, 1391, 174 USPQ 259, 260 (CCPA 1972); 37 CFR § 1.192(c)(7)(1997).

Claims 13, 17-19, 23 and 24

Shou (figure 3) discloses a gate which extends beyond a recessed strangulation region (S1) and a gate which is not shown as extending beyond common p-type semiconductor layer PL1.

The appellants argue that "[t]he limitation not described in the prior art is that the length of the second gate electrode, from the third edge to the first end thereof, is greater than the length of the first gate electrode from the fourth edge to the first end thereof" (brief, page 7). This argument, applied to the appellants' figure 24, is that the prior art does not describe a length of gate electrode 30H, from the edge of ordinary region OR2 which it intersects (third edge) to what appears in as the upper end of gate electrode 30H,[3] which is greater than length x of gate electrode 20, which is the length

[3] Figure 24 is a plan view of the semiconductor device.

from the edge of ordinary region OR1 which it intersects (fourth edge) to what appears as the upper end of gate electrode 20. The appellants argue that "if *Shou et al.* recognized the problem of not providing an end cap [i.e., an extension of the gate beyond PL1], *Shou et al.* would have described the edge of the gate electrode G as projecting beyond the edge portion of the active region PL1. However, no description is made within the body of the patent and neither is anything shown in Figure 3 of *Shou et al.*" (brief, page 8).

The examiner argues that "one skilled in the art would understand that the ordinary gate must necessarily extend at least some distance onto the surrounding oxide region (i.e., that end caps must necessarily be present on the ordinary gate as well as the recessed gate); otherwise the source/drain regions of the ordinary region would be inclined to short and the transistor would not operate as intended" (answer, pages 4-5).

The examiner's argument is plausible, particularly in view of the appellants' acknowledgment that it was known in the art to use end caps so that the forward end portions of gate electrodes are not located on active areas even if the gate electrodes are rounded due to corrosion by etching or the like to partially reduce their lengths (specification, page 2, lines 5-7). Because

the examiner's argument is plausible and has not been challenged by the appellants, we accept it as being correct.

Moreover, Bergemont discloses that it was conventional to make end caps sufficiently long that the channel length is greater than an acceptable minimum required to prevent current leakage caused by misalignment or rounding of a gate electrode and a field oxide island onto which the gate electrode extends (page 1, lines 19-33). Hence, even if Shou's ordinary region gate does not necessarily have an end cap, Bergemont would have fairly suggested an end cap to one of ordinary skill in the art to prevent current leakage.

The appellants argue that Bergemont would not have suggested lengths of end caps which are different from one another (brief, pages 10-11).

The examiner argues that because Shou's gates in the ordinary and strangulation regions form a line (figure 3), the distance from the active area in the strangulation region to the end of the gate necessarily is longer than the distance from the active area in the ordinary region to the end of the gate (answer, pages 11-12). The examiner also argues that because Shou's ordinary region gate necessarily has an end cap, or because Bergemont and the admitted prior art would have fairly

suggested such an end cap to one of ordinary skill in the art, the end of Shou's strangulation region gate which is in line with the ordinary region gate extends beyond the non-recessed region, i.e., the length of the strangulation region gate is greater than the lengths of the first and second edges as recited in the appellants' claims 17 and 23. *See id.*

Because the examiner's reasoning is plausible and has not been challenged by the appellants, we accept it as being correct. Moreover, Bergemont's teaching that rounding of field oxide islands which extend into active regions tends to cause current leakage (page 1, lines 19-33) would have fairly suggested, to one of ordinary skill in the art, extending the length of Shou's gate onto the field oxide island in the strangulation region sufficiently to prevent this current leakage, with the optimum length being determined through no more than routine experimentation. *See In re Boesch*, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980); *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Thus, contrary to the appellants' argument (brief, page 9), the applied prior art would have rendered *prima facie* obvious, to one of ordinary skill in the art, aligned end edges of Shou's strangulation region and ordinary region electrodes as required by the appellants' claims 18 and 24, and a

strangulation region gate electrode length which is greater than the strangulation region edge lengths as required by the appellants' claims 17 and 23.[4]

For the above reasons we conclude that a *prima facie* case of obviousness of the semiconductor device and the method for making it claimed in the appellants' claims 13, 17-19, 23 and 24 over Shou in view of Bergemont has been established and has not been effectively rebutted by the appellants. Accordingly, we affirm the rejection of these claims.

Claims 14-16 and 20-22

The outer edges of Shou's strangulation region are in a line (figure 3). The appellants argue that the applied prior art would not have suggested 1) making one edge of the strangulation region longer than the other edge, and making the strangulation region gate electrode length greater than the length of the shorter edge as required by the appellants' claims 14 and 20,

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[4] Bergemont shows a field oxide island having edges (figure 1A) as recited in the appellants' claims, but teaches that the edges actually are rounded (page 1, lines 19-21; figures 1B and 1C). Bergemont teaches that "[t]he field oxide rounding effect is inherent to the type of field isolation and photolithographic process used" (page 1, lines 21-22). Thus, it reasonably appears that the rounded field oxide islands shown by Shou (figure 3) and Bergemont have edges as that term is used by the appellants.

2) making the length of the strangulation region gate electrode equal to the sum of the ordinary region gate end cap length and the length of the shorter edge as required by the appellants' claims 15 and 21, and 3) making the strangulation region gate electrode length equal to the sum of the ordinary region gate end cap length and a length from the bottom of the strangulation region recess to an intersection of the strangulation region gate electrode and an imaginary line connecting the longer edge and the shorter edge as required by the appellants' claims 16 and 22 (brief, page 12).

The examiner points out that Jassowski discloses a first edge (labeled E1 by the examiner in figure 2) and, parallel thereto, a shorter second edge (E2). A third edge (E3), past which gate G4 extends, is perpendicular to edges E1 and E2, and these three edges form a recess. The examiner acknowledges that the distance which gate G4 extends into the recess is much less than the length of second edge E2, and argues that Jassowski's disclosure in combination with Shou's disclosure that the end edge of the strangulation region gate is in line with the end edge of the end cap of the ordinary region's gate and, therefore, extends beyond the edges of the strangulation region, and Bergemont's disclosure that increasing the length that a gate

extends onto a field oxide island prevents current leakage, would have fairly suggested, to one of ordinary skill in the art, extending a gate in a recessed region by any degree between those disclosed by Jassowski and Shou, including the extensions required by the appellants' claims 14-16 and 20-22, in order to avoid current leakage, with the particular degree of extension being determined through no more than routine experimentation (answer, pages 6-8). The examiner also points out that the length of Jassowski's edge E5 is less than that of E1, and that gate G1 close to edge E5 extends beyond that edge by the length of the end cap of ordinary region gate G2 (answer, page 7). The examiner argues that this disclosure, in combination with the above-discussed disclosure of Bergemont, would have fairly suggested, to one of ordinary skill in the art, whether a gate is at a corner region like edge E5 or is in a recessed region having unequal parallel edge lengths like edges E1 and E2, extending the gate such that its end edge is in line with the end edge of an ordinary region gate's end cap to prevent shorting caused by misalignment or rounding. *See id.* The examiner argues that the specific application intended for the active region "dictates various conventional details such as the channel width and length, which in turn, dictates the length and spacing

requirements for the three edges of the recessed portion and the layout constraints for the circuit cell" (answer, page 7).

The appellants argue that each of Shou, Bergemont and Jassowski does not disclose the limitations recited in the appellants' claims 14-16 and 20-22 (brief, pages 13-14). This argument is deficient in that the appellants are attacking the references individually when the rejection is based on a combination of references. *See In re Keller*, 642 F.2d 413, 426, 208 USPQ 871, 882 (CCPA 1981); *In re Young*, 403 F.2d 754, 757-58, 159 USPQ 725, 728 (CCPA 1968).

The examiner has provided a plausible explanation as to why the applied references, in combination, together with the appellants' admitted prior art, would have fairly suggested, to one of ordinary skill in the art, the relative gate and edge lengths recited in each of the appellants' claims 14-16 and 20-22. The appellants have not addressed the examiner's reasoning and provided evidence or reasoning to the contrary.

We therefore conclude that the semiconductor device and method for manufacturing a semiconductor device claimed in the appellants' claims 14-16 and 20-22 would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103. Consequently, we affirm the rejection of those claims.

DECISION

The rejections under 35 U.S.C. § 103 of claims 13, 17-19, 23 and 24 over Shou in view of Bergemont, and claims 14-16 and 20-22 over Shou in view of Bergemont and Jassowski, are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

EDWARD C. KIMLIN
Administrative Patent Judge

BRADLEY R. GARRIS
Administrative Patent Judge

TERRY J. OWENS
Administrative Patent Judge

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Board of Patent Appeals and Interferences
Docketing Notice

Application 09/114,203 was received from the Technology Center at the Board on September 15, 2003 and has been assigned Appeal No: 2003-2132.

A review of the file indicates that the following documents have been filed by appellant:

Appeal Brief filed on: March 10, 2003
Reply Brief filed on: None
Request for Hearing filed on: None

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